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(54) Carry look-ahead addition circuits

(57) A method of designing an addition circuit, and an addition circuit designed according to the method are described. The design technique is optimised to facilitate design of an addition circuit of minimum depth. The design technique takes into account the number of logical stages of the addition circuit and the manner in which those stages are connected by spanning paths to create fan-out nodes. The number of fan-out nodes per level can be optimised.

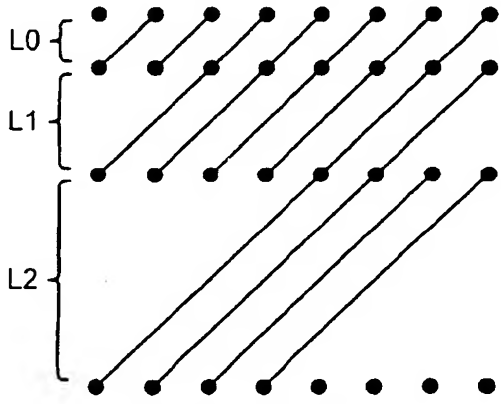

FIG. 3a [1,1,1]

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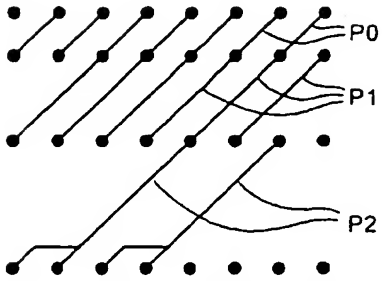
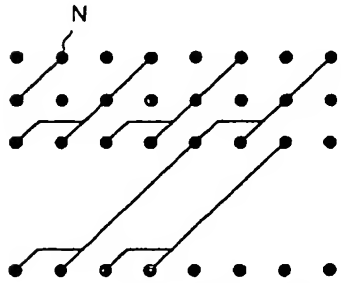
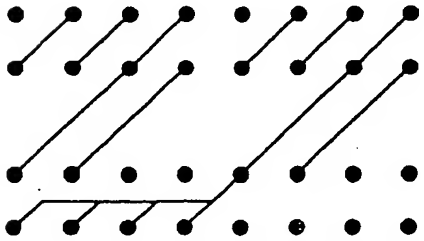


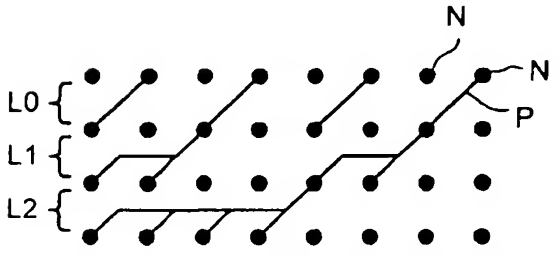
[2,1,1] FIG. 3b



[2,2,1] FIG. 3c



[4,1,1] FIG. 3d



[4,2,1] FIG. 3e

Description

[0001] The present invention relates to addition circuits for adding a binary number A to a binary number B. The present invention relates particularly but not exclusively to addition circuits designed to meet particular process or application criteria.

[0002] A variety of different addition circuits are known. One basic example is illustrated in Figure 1. The binary number A is represented as a series of bits a_i where i is the binary weight of the bit a_i and increases from the value zero for the least significant bit of A in steps of one to the value of the most significant bit of A. The binary number B is a series of bits b_i where i is the binary weight of the bit. The summation of the numbers A and B is represented by the binary number S which is a series of bits s_i where i is the binary weight of the bit, and C_8 which is the msb of the sum.

[0003] The bit a_0 and the bit b_0 are supplied as inputs to an AND gate 2_0 which produces the bit generate g_0. The bit a_0 and the bit b_0 are also supplied as inputs to an XOR gate 4_0 which produces s_0 as its output. The bit a_1 and the bit b_1 are supplied as inputs to an XOR gate 4_1 which produces the first bit propagate signal p_1. The bit generate signal g_0 and the first bit propagate signal p_1 are supplied as inputs to an XOR gate 24_1 which produces the bit s_1. The bit a_1 and the bit b_1 are also supplied as inputs to an OR gate 6_1 which supplies its output as a first input to an AND gate 8_1. The second input of the AND gate 8_1 is received from the output of the AND gate 2_0. The output of the AND gate 8_1 provides a first input to an OR gate 10_1. The second input to the OR gate 10_1 is received from an AND gate 2_1 which receives as inputs the bit a_1 and the bit b_1. The bit a_2 and the bit b_2 are supplied as inputs to an XOR gate 4_2 which provides its output as a first input to a XOR gate 24_2. The second input to the XOR gate 24_2 is provided by the output of the OR gate 10_1. The output of the XOR gate 24_2 provides the bit s_2. The bit a_2 and the bit b_2 are also combined in an OR gate 6_2 to produce a first input to an AND gate 8_2 which receives as a second input the output from the OR gate 10_1. The output from the AND gate 8_2 supplied as a first input to a OR gate 10_2. The second input to the OR gate 10_2 is supplied by a AND gate 2_2 which receives as an input the bits a_2 and b_2. The output of the OR gate 10_2 is supplied as a first input to a XOR gate 24_3. The second input to the XOR gate 24_3 is supplied by the output of an XOR gate 4_3 which receives as inputs the bit a_3 and the bit b_3. The output of the XOR gate 24_3 provides the bit s_3. An AND gate 2_3 also receives the bits a_3 and b_3 and provides its output as a first input to a OR gate 16_3. The second input to the OR gate 16_3 is provided by an AND gate 14_3 which receives as a first input the output from the AND gate 2_2 and as a second input the output from an OR gate 6_3 which receives as inputs the bit a_3 and bit b_3. The output from the OR gate 6_3 is also provided as a first input to an AND gate 12_3 which receives as a second input the output from the OR gate 6_2. The output from the AND gate 12_3 is supplied as a first input to an AND gate 8_3 which receives as a second input the output from the OR gate 10_1. The output from the AND gate 8_3 and the output from the OR gate 16_3 are combined in an OR gate 10_3. A XOR gate 24_4 receives as a first input the output from the OR gate 10_3 and as a second input the output from an XOR gate 4_4 which receives as inputs the bit a_4 and the bit b_4. The XOR gate 24_4 produces the bit s_4. An OR gate 6_4 receives an inputs the bit a_4 and bit b_4 and provides its output as a first input to an AND gate 8_4. The AND gate 8_4 receives as its second input the output from the OR gate 10_3 and provides its output to a OR gate 10_4. The other input to the OR gate 10_4 is provided by an AND gate 2_4 which receives as inputs the bit a_4 and the bit b_4. An XOR gate 24_5 produces the bit s_5 and receives as a first input the output from the OR gate 10_4 and receives as a second input the output from an XOR gate 4_5 which receives as inputs the bit a_5 and the bit b_5. An AND gate 12_5 receives as a first input the output from the OR gate 6_4 and an output from an OR gate 6_5 which receives as inputs the bit a_5 and the bit b_5. An OR gate 16_5 receives as a first input the output from an AND gate 2_5 which receives as inputs the bit a_5 and the bit b_5 and as a second input receives the output from an AND gate 14_5 which itself receives as inputs the output from the AND gate 2_4 and the output from the OR gate 6_5. The output from the AND gate 12_5 is combined with the output from the OR gate 10_3 in an AND gate 8_5 to produce a first input to a first OR gate 10_5. The second input to the OR gate 10_5 is provided by the output from the OR gate 16_5. The output from the OR gate 10_5 is provided as a first input to the XOR gate 24_6. The XOR gate 24_6 receives as a second input the output from the XOR gate 4_6 which receives as inputs the bit a_6 and the bit b_6. The XOR gate 24_6 produces as an output the bit s_6. An OR gate 6_6 receives as its inputs the bit a_6 and the bit b_6 and supplies its output as a first input to an AND gate 12_6. The second input to the AND gate 12_6 is supplied by the output of the AND gate 12_5 and the output of the AND gate 12_6 is supplied as a first input to an AND gate 8_6. The output from the OR gate 6_6 is supplied as a first input to an AND gate 14_6. The AND gate 14_6 receives as a second input the output from the OR gate 16_5 and provides an output signal to a first input of an OR gate 16_6. The second input to the OR gate 16_6 is supplied by an AND gate 2_6 which receives as inputs the bit a_6 and the bit b_6. The AND gate 8_6 which receives as a first input the output from the AND gate 12_6 receives as a second input the output from the OR gate 10_3 and provides its output as a first input to an OR gate 10_6. The second input to the OR gate 10_6 is provided by the output of the OR gate 16_6. The output of the OR gate 10_6 is provided as a first input to an XOR gate 24_7. The XOR gate 24_7 receives as a second input the output from an XOR gate 4_7 which receives as inputs the bit a_7 and the bit b_7. The XOR gate 24_7 produces the bit s_7. The bit a_7 and the bit b_7 are combined in an OR gate 6_7

to produce a first input to an AND gate 18_7 which receives as a second input the output from the OR gate 6_6. The output from the OR gate 6_7 is supplied as a first input to an AND gate 20_7. The AND gate 20_7 receives as a second input the output from the AND gate 2_6. The output from the AND gate 20_7 is supplied as a first input to an OR gate 22_7. The second input to the OR gate 22_7 is provided by a AND gate 2_7 which receives as its inputs the bit signal a_7 and the bit signal b_7. An AND gate 14_7 receives as its inputs the output from the AND gate 18_7 and the output from the OR gate 16_5 and provides its output as a first input to an OR gate 16_7. The second input to the OR gate 16_7 is supplied by the output of the OR gate 22_7. The output of the OR gate 16_7 is provided as a first input to an OR gate 10_7. An AND gate 12_7 receives as its inputs the output from the AND gate 12_5 and the output from the AND gate 18_7. The output from the AND gate 12_7 is supplied as a first input to the AND gate 8_7. The AND gate 8_7 receives as a second input the output from the OR gate 10_3. The output from the AND gate 8_7 is supplied as a second input to the OR gate 10_7. The output of the OR gate 10_7 produces the last carry value c_8.

[0004] An addition circuit which can quickly change between producing an output value A+B and output value A+B+1 or which can simultaneously provide an output value A+B and an output value A+B+1 is described in our earlier GB Patent Application No. 9813328.3.

[0005] The addition circuitry described in that application has a plurality of addition paths, with each addition path having inputs for receiving respectively bits a_i, b_i of the first and second binary numbers and output means for producing respectively bits s_i, s'_i of third (A+B) and fourth (A+B+1) binary numbers.

[0006] By modification to the output means, the circuit can be configured to provide a number of different useful outputs, such as A+B or A+B+1; A+B and A+B+1; A-B and B-A; A-B or B-A; and modulus A-B. Thus, the circuit has a number of different useful applications.

[0007] Each addition path has a number of logical nodes in the depth direction of the circuit (input to output). Each set of nodes arranged widthwise of the circuit (that is in the direction of bit significance) forms a logical stage. Each adjacent pair of addition paths defines a column. An addition circuit of so-called "minimum depth" has the minimum number of logical stages which are required to add together the binary numbers according to their length n. Clearly, the greater the length n of binary numbers to be added, the higher is the number of stages even in a "minimum depth" circuit. In developing a minimum depth circuit, clearly constraints are imposed on how the logical nodes can be interconnected. In GB Application No. 9813328.3, the circuit is designed so that each logical node is connected to as many logical nodes in the subsequent logical stage as possible. This connection is made via the addition path for the node and by one or more spanning path which crosses at least one column. The number of nodes in a subsequent stage to which a node of the preceding logical stage is connected by spanning paths is termed herein "fan-out". Thus, the circuit of the earlier application is designed with so-called maximum fan-out. This has the advantage of minimising the number of wires which are required to make the circuit, but has the disadvantage that delays between logical states are incurred as a result of the capacitance introduced by the large number of gates connected to particular wires, particularly in the later logical stages.

[0008] Another possibility is to interconnect a node of a logical stage to a unique single node of a subsequent stage, which has the advantage of reducing fan-out (to a fan-out of 1), but the disadvantage of requiring a large number of wires which increases the space requirement for the circuit.

[0009] It would be desirable to be able to design an addition circuit to accommodate a number of different process and application criteria. In particular it would be desirable to facilitate design of an addition circuit of minimum depth.

[0010] According to the present invention there is provided an addition circuit for adding together two binary numbers (A,B) having a length of n bits, comprising:

an array of logical nodes which are arranged so that each set of logical nodes extending widthwise of the circuit form a logical stage and each set of nodes extending depthwise of the circuits forms an addition path, with each pair of adjacent addition paths forming a column;

spanning paths arranged to interconnect selected logical nodes so that adjacent logical stages are connected via an interconnection level, each spanning path extending from a node in one stage across at least one column being connected to a number f of fan-out nodes in a subsequent stage, the circuit having the following configuration parameters:

i) for each interconnection level the number f of fan-out nodes lies in the range 1 to 2^j, where j is the interconnection level index lying between 0 and m, 2^j is the maximum fan-out number for that level, and there are m+2 logical stages;

ii) the fan-out f of nodes at each level is always no greater than the number f of fan-out nodes at a subsequent level;

iii) the number of columns across which a spanning path extends within an interconnection level is 2^j;

wherein at least one level has a fan-out number $f < 2^j$ and at least one level has a fan-out number $f > 1$.

[0011] By defining a number of criteria for the addition circuit in terms of the configuration parameters referred

to above, it is possible to design the addition circuit to suit the particular requirements at hand. That is, it allows designs to be constructed with fewer spanning wires and/or lower fan-out, without significantly compromising speed requirements for a given circuit depth. The configuration parameters allow a number of design trade-offs to be considered each time resulting in an optimised addition circuit for the particular instant application.

[0012] The invention is particularly useful in the context of minimum depth addition circuits. For an addition circuit of minimum depth, the number m+2 of logical stages is derived from the following equations:

$$n = 2^{m+1}$$

(where n is a binary order), and

$$n_{b0} = 2^{m+1}$$

(where n is not a binary order and where n_{b0} is the next largest binary order after n).

[0013] In the described embodiment, each logical node comprises at least one logic gate which receives at least two signals representing bits of the same significance i in the binary numbers a, b to be added.

[0014] Each spanning path can convey one or more signal from a node of one significance in one logical stage to a node of a different significance in a subsequent logical stage.

[0015] Another aspect of the invention provides a method of designing an addition circuit for adding together two binary numbers (A,B) each of bit length n, the method comprising:

determining the number (m+2) of logical stages in the addition circuit according to the following:

for bit length n of a binary order, $n = 2^{m+1}$ and for bit lengths which are not binary orders $n_{b0} = 2^{m+1}$ where n_{b0} is the next largest binary order after n;

for each of said logical stages allocating a set of virtual nodes, said virtual nodes forming potential addition paths depthwise of the circuit and adjacent addition paths forming a column;

determining for each logical stage its expected input capacitance; and

defining spanning paths wherein the spanning paths constitute an interconnection level between adjacent logical stages, wherein definition of the spanning paths is carried out in accordance with the following configuration parameters and depending on the expected input capacitance of each stage:

i) for each interconnection level the number f of fan-out nodes in a subsequent stage to which a node of a preceding stage is connected lies in the range 1 to 2^j, where j is the interconnection level index lying between 0 and m and 2^j is the maximum fan-out number for that level,

ii) the fan-out f of nodes at each level is always no greater than the fan-out f of nodes at a subsequent level,

iii) the number of columns across which a spanning path extends within an interconnection level is 2^j,

wherein at least one level has a fan-out number $f < 2^j$ and at least one level has a fan-out number $f > 1$.

[0016] A number of different specific examples are possible. By way of illustration, the following particular examples are mentioned, but this is in no way a comprehensive list of all of the possible options.

[0017] An addition circuit wherein the fan-out f=1 for more than one level.

[0018] An addition circuit wherein f=1 for all levels except the mth level.

[0019] An addition circuit wherein at least one level has maximum fan-out $f=2^j$ where j is not equal to m.

[0020] An addition circuit where the fan-out f=2 for at least two levels.

[0021] For a better understanding of the present invention and to understand how the same may be brought into effect reference will now be made by way of example only to the accompanying figures in which:

Figure 1 illustrates prior art circuitry for producing A+B in more detail;

Figure 2 illustrates the circuit of Figure 1 but labelled to clearly denote the layout of the logical nodes;

Figure 3a to 3e are node diagrams for addition circuits where n=8;

Figures 4a to 4e illustrates addition circuits implementing node diagrams of Figures 3a to 3d respectively; and

Figures 5a through 5n are node diagrams for addition circuits where n=16.

[0022] Firstly, Figure 2 will be used to describe the overall layout of the known addition circuit already illustrated in Figure 1. The bit significance 0 ... 7 is labelled for each addition path moving from the right hand side to the left hand side widthwise of the circuit of Figure 2. The circuit has a plurality of logical nodes which are labelled according to the following notation:

Ni,k where i is the bit significance of the node and k is an index defining the depth of the node within the addition circuit in a manner which will become clearer in the following.

[0023] The nodes N are arranged so that each set of logical nodes extending widthwise of the circuit forms a logical stage. That is, the nodes N0,0 ... N7,0 form logical stage k=0, the nodes N1,1, N3,1, N5,1 and N7,1 form the logical stage k=1; the nodes N2,2, N3,2, N6,2,

N7,2 form the logical stage k=2; and the nodes N4,3 ... N7,3 form logical stage k=3.

[0024] Depthwise of the circuit, each set of nodes forms an addition path. Each pair of adjacent addition paths constitutes a column labelled C1 to C7 in Figure 2. The logical stages are interconnected by interconnection levels which are marked L0 to L2 in Figure 2. Each interconnection level L0 to L3 comprises a number of spanning paths which are wires connecting a node N in a preceding stage to one or more node in a subsequent stage. Each spanning path can extend across one or more columns and comprise one or more wires for transferring one or more signals. In Figure 2, the interconnection level L0 has spanning paths P0,0, P2,0, P4,0 and P6,0. P0,0 conveys a single signal from bit significance 0 to bit significance 1 across column C1. P2,0 conveys two signals from bit significance 2 to bit significance 3 across column 3. Similarly P4,0 and P6,0 each convey two signals across a single column. The spanning paths in level 1, P1,1 and P5,1 respectively cross two columns. Also, they connect the node of stage 1 to two nodes of stage 2. The number of nodes in a subsequent stage to which a node of a preceding stage is connected by spanning paths is termed herein "fan-out". Of course, there are also a number of connections between modes vertically along an addition path. Thus, the interconnection level L1 has a fan-out of 2. Applying the same principles, it can be seen that the interconnection level L2 has a fan-out of 4, connecting the node N3,2 in stages to each of the four nodes N4,3 ... N7,3 in stage 3.

[0025] The composition of each node in terms of its logical gates, and the function of those logical gates can be seen by comparing Figure 2 with Figure 1. For example, the node N2,0 comprises the two logic gates 6_2 and 2_2. As another example, the node N5,1 comprises the three logic gates 12_5, 14_5 and 16_5. It will be appreciated that the nodes of the first stage each include an Exclusive OR gate 4_0 ... 4_7, and that the nodes of the first stage each include an Exclusive OR gate 24_0 ... 24_7.

[0026] Figure 3e illustrates a node diagram for the circuit of Figure 2. In Figure 3e, a complete array of eight by four "virtual" nodes is illustrated, each node being represented by a black dot.

[0027] The spanning paths P are denoted by black lines. In the diagram of 3e, it is easier to see that the fan-out for interconnection level L0 is 1, the fan-out for interconnection level L1 is 2 and the fan-out for interconnection level L2 is 4. The circuit is therefore defined by the notation [4,2,1], which is the fan-out for each interconnection level, taking the lattermost interconnection level first.

[0028] As already mentioned, a problem which exists with this circuit is the high fan-out for the last and last but one level, which imposes signal delays through the interconnection levels. One way of avoiding this would be to construct a circuit along the lines illustrates in the node diagram of Figure 3a. In that diagram, it can readily be seen that each interconnection level L0, L1 and L2 has a fan-out of 1. However, what is also clearly evident is the number of wires which are required to implement the circuit. It will be appreciated that the number of wires is related to the number of spanning paths P.

[0029] The inventor has determined that there are a number of other design options which, for a bit length N = 8 and a minimum depth addition circuit are illustrated in Figures 3b, 3c and 3d. In each of those figures, a complete array of eight by four "virtual" nodes is illustrated, each node N being represented by a black dot. Scanning paths P are denoted by a black line. The addition circuits of Figures 3b, 3c and 3d share the following characteristics.

i) For each interconnection level Lj, the number f of fan-out nodes lies in the range 1 to 2^j. j denotes the interconnection level index. In the addition circuits of Figures 3b, 3c and 3d, j is 0,1 or 2. 2^j is the maximum fan-out number for a particular level.

ii) The number f of fan-out nodes at each level is always no greater than the number f of fan-out nodes at a subsequent level.

[0030] Thus, in Figure 3b the fan-out for levels L0 and L1 is 1, and the fan-out for level L2 is 2. In Figure 3c the fan-out for level L0 is 1 and the fan out for levels L1 and L2 is 2. In Figure 3d, the fan-out for levels L0 and L1 is 1, and the fan-out for level L2 is 4.

iii) the number of columns across which a spanning path extends within an interconnection level is 2^j. Thus, for an eight bit adder as illustrated in Figures 3b, 3c and 3d the spanning paths P0 in level L0 cross one column, the spanning paths P1 in level L1 cross two columns, and the spanning paths P2 at level L2 cross four columns.

[0031] The addition circuits of Figures 3b, 3c and 3d also share the parameters that at least one level has a fan-out number less than its maximum, and at least one level has a fan-out number greater than one. By allowing these criteria to be varied, addition circuits can be designed in accordance with the required parameters of any particular application. Where space is a significant consideration, the number of wires can be reduced by using increased fan-out at different levels. Where capacitive delays are a problem, these can be reduced by reducing fan-out where possible, and increasing the number of levels where fan-out is less than its maximum.

[0032] Figures 4b, 4c and 4d represent the circuit implementations of the node diagrams of Figures 3b, 3c and 3d respectively. In each of these circuit diagrams, the nodes marked N correspond to the nodes N illustrated by black dots connected by black lines in Figures 3b, 3c and 3d. The black dots in the node array diagrams of Figures 3b, 3c and 3d which are not connected by black lines do not of course find an equivalent in the circuit diagrams of Figures 4b, 4c and 4d. The configura-

tion of logic gates required for each node can readily be determined by selecting an appropriate configuration from the circuit of Figure 2 depending on the number of input signals required to be combined at the node, and whether these have come from a spanning path or an addition path of the same bit significance.

[0033] The principles of the invention can readily be extended to addition circuits for adding binary numbers of different lengths. The invention is predominantly concerned with so-called minimum depth addition circuits, where the number of stages in the addition circuit is determined according to the following criteria:

for bit lengths n of a binary order, the number m+2 of logical stages is derived from the following equation: $n = 2^{m+1}$, and

for bit lengths n which are not binary orders, the number m+2 of logical stages is derived from the following equation: $n_{b0} = 2^{m+1}$ where nb0 is the next largest binary order after n.

[0034] As will be apparent, in the preceding example m = 2, the number of interconnection levels (index j) is m+1 = 3 and the number of logical stages (index k) is m+2 = 4. Figures 5a to 5n illustrate possible addition circuits where N = 16 and m = 3. Figures 5b to 5m represent circuits in accordance with embodiments of the present invention, that is circuits which follow the configuration parameters discussed above.

[0035] In designing an addition circuit using the node array diagrams illustrated in Figures 3 and 5 and conforming to the above-mentioned criteria, it will be appreciated that those zones which are empty of spanning paths can quickly be identified. Of course, it is not necessary to implement a logical node with logic circuitry where it is not connected to any other node.

[0036] A method of designing an addition circuit will now be described. The binary length n of the numbers to be added is first specified. Then, the number of logical stages in the addition circuit is determined according to the above defined criteria for a minimum depth addition circuit. The required output drive strength of the addition circuit is established, and this defines the size of the logic gates requires to implement the nodes of the final stage. The size of the logic gates used to implement the nodes of the final stage determines the input capacitance of that stage. At this point, the design options available according to the configuration parameters of the present invention can be considered to provide a number of different options for the addition circuit. For each or a selected group of these options, the capacitance of the spanning paths in the interconnection level to the final stage can be calculated. The choice of a spanning configuration in terms of the number of wires vs the extent of fan-out determines the size of logic gates at the driving level, which in turn determines the input capacitance as seen by the preceding level. Thus, a recursive design method is implemented to determine an optimum addition circuit for the application in hand.

[0037] The present invention thus provides a number of different design options for addition circuits which allow a designer more freedom than has hitherto been the case in designing addition circuits.

Claims

1. An addition circuit for adding together two binary numbers (A,B) each having a length of n bits, comprising:

   an array of logical nodes which are arranged so that each set of logical nodes extending widthwise of the circuit form a logical stage and each set of nodes extending depthwise of the circuits forms an addition path, with each pair of adjacent addition paths forming a column;
   spanning paths arranged to interconnect selected logical nodes so that adjacent logical stages are connected via an interconnection level, each spanning path extending from a node in one stage across at least one column being connected to a number f of fan-out nodes in a subsequent stage, the circuit having the following configuration parameters:

   i) for each interconnection level the number f of fan-out nodes lies in the range 1 to 2^j, where j is the interconnection level index lying between 0 and m, 2^j is the maximum fan-out number for that level, and there are m+2 logical stages;

   ii) the fan-out f of nodes at each level is always no greater than the number f of fan-out nodes at a subsequent level;

   iii) the number of columns across which a spanning path extends within an interconnection level is 2^j;

   wherein at least one level has a fan-out number $f < 2^j$ and at least one level has a fan-out number $f > 1$.

2. An addition circuit as claimed in claim 1, wherein for bit lengths N of a binary order the number (m+2) of logical stages is derived from the following equation:

$$n = 2^{m+1}.$$

3. An addition circuit according to claim 1, wherein for bit lengths N which are not binary orders, the number (m+2) of logical stages is derived from the following equation:

$$n_{bo} = 2^{m+1}$$

where n_{bo} is the next largest binary order after n.

4. An addition circuit according to claim 1, 2 or 3, wherein each logical node receives at least two signals representing bits of the same significance (i) in the binary numbers (A,B) to be added, and comprises at least one logic gate.

5. An addition circuit according to claim 1, 2, 3 or 4, wherein each spanning path conveys one or more signal from a node of one significance in one logical stage to a node of a different significance in a subsequent logical stage.

6. An addition circuit according to any preceding claim wherein the fan-out f = 1 for more than one level.

7. An addition circuit according to claim 6, wherein f = 1 for all levels except the mth level.

8. An addition circuit according to any of claims 1 to 5, wherein at least one level has maximum fan-out (f = 2^i) where j = m.

9. An addition circuit according to any of claims 1 to 5, where the fan-out f = 2 for at least two levels

10. A method of designing an addition circuit for adding together two binary numbers (A,B) each of bit length n, the method comprising:

determining the number (m+2) of logical stages in the addition circuit according to the following:
for bit length n of a binary order, $n = 2^{m+1}$
and for bit lengths which are not binary orders $n_{b0} = 2^{m+1}$ where n_{b0} is the next largest binary order after n;
for each of said logical stages allocating a set of virtual nodes, said virtual nodes forming potential addition paths depthwise of the circuit and adjacent addition paths forming a column;
determining for each logical stage its expected input capacitance; and
defining spanning paths wherein the spanning paths constitute an interconnection level between adjacent logical stages, wherein definition of the spanning paths is carried out in accordance with the following configuration parameters and depending on the expected input capacitance of each stage:

i) for each interconnection level the number f of fan-out nodes in a subsequent stage to which a node of a preceding stage is connected lies in the range 1 to 2^j, where j is the interconnection level index lying between 0 and m and 2^j is the maximum fan-out number for that level,

ii) the fan-out f of nodes at each level is always no greater than the fan-out f of nodes at a subsequent level,

iii) the number of columns across which a spanning path extends within an interconnection level is 2^j,

wherein aleast one level has a fan-out number $f < 2^j$ and at least one level has a fan-out number $f > 1$.

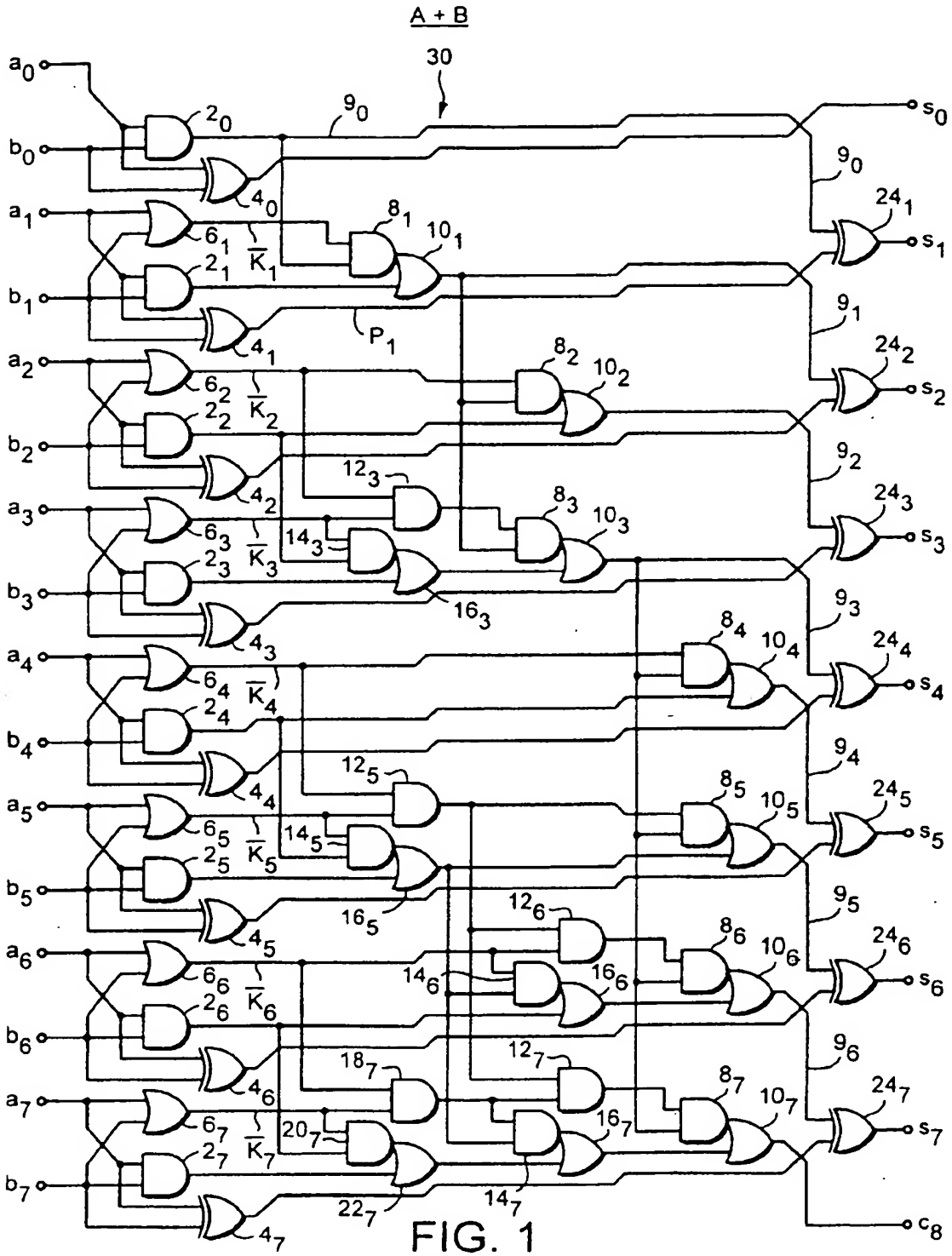


FIG. 1
PRIOR ART

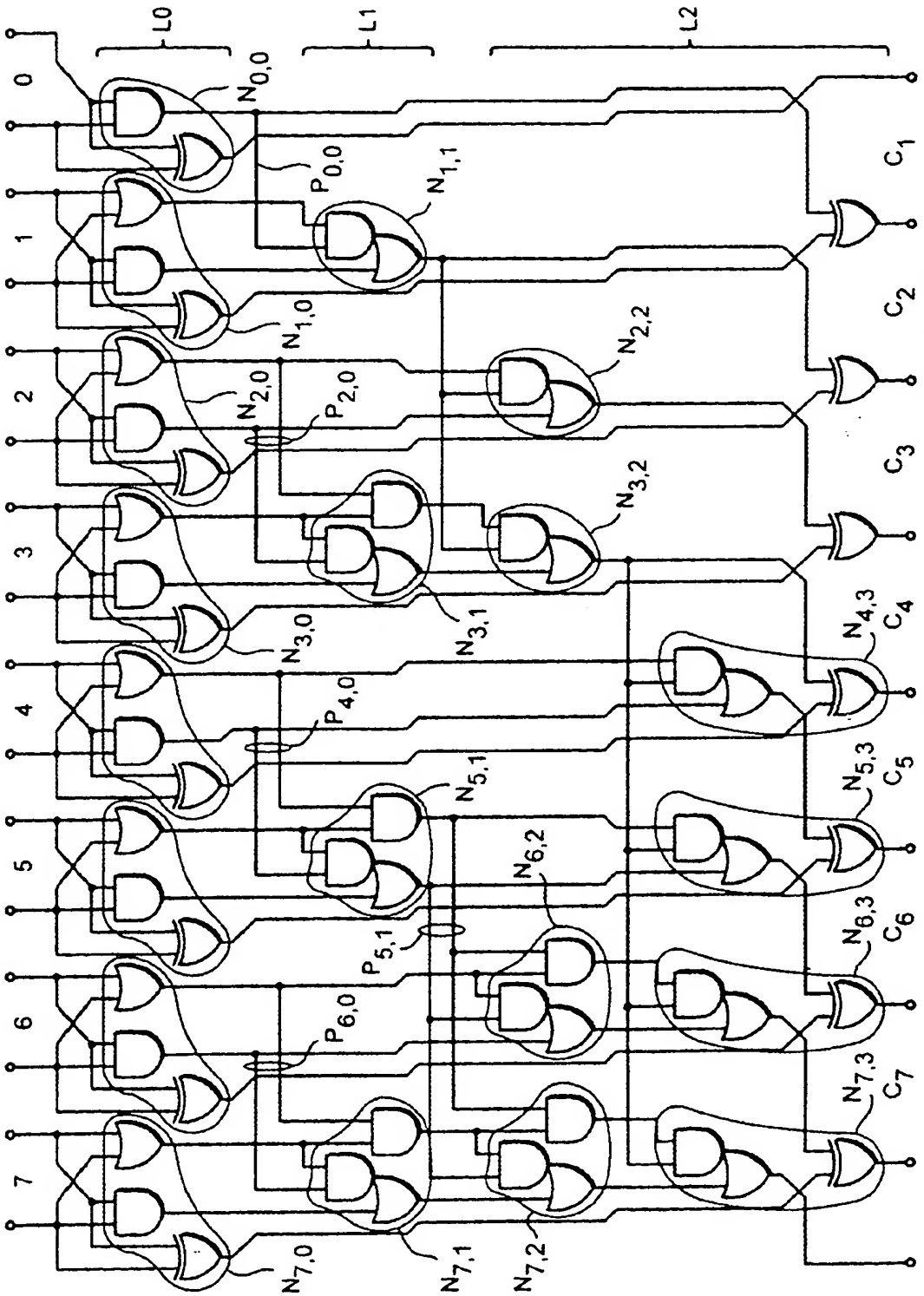

L0
L1
L2
0
1
2
3
4
5
6
7
$N_{0,0}$
$P_{0,0}$
$N_{1,1}$
$N_{1,0}$
$N_{2,0}$
$P_{2,0}$
$N_{2,2}$
$N_{3,2}$
$N_{3,0}$
$N_{3,1}$
$P_{4,0}$
$N_{4,3}$
$N_{5,1}$
$N_{5,3}$
$N_{6,2}$
$P_{5,1}$
$P_{6,0}$
$N_{6,3}$
$N_{7,3}$
$N_{7,0}$
$N_{7,1}$
$N_{7,2}$
C_1
C_2
C_3
C_4
C_5
C_6
C_7
[4,2,1]

FIG. 2

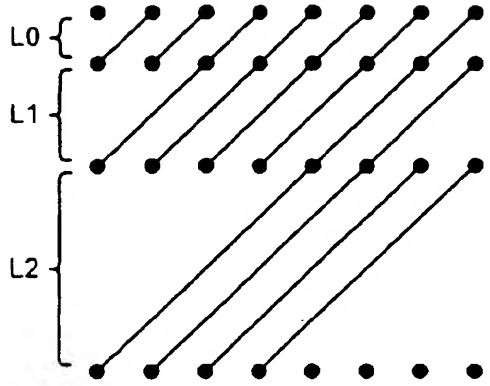
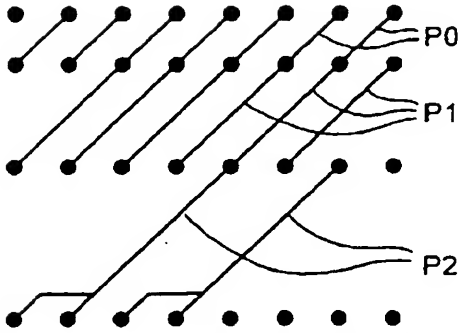
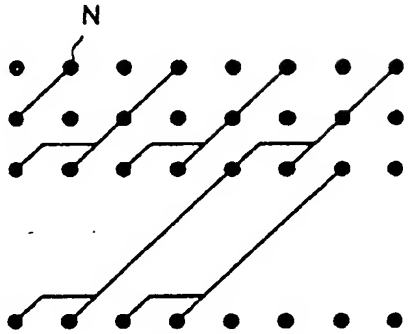


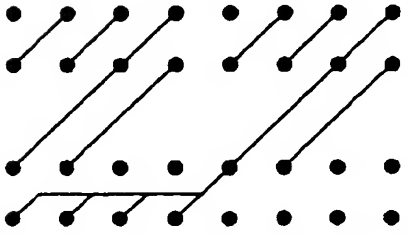
FIG. 3a [1,1,1]



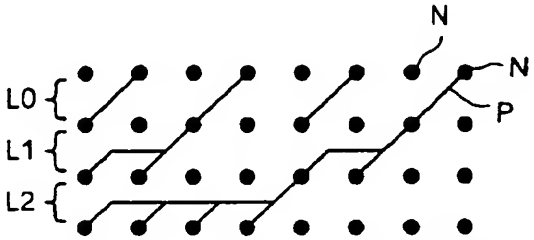
[2,1,1] FIG. 3b



[2,2,1] FIG. 3c



[4,1,1] FIG. 3d



[4,2,1] FIG. 3e

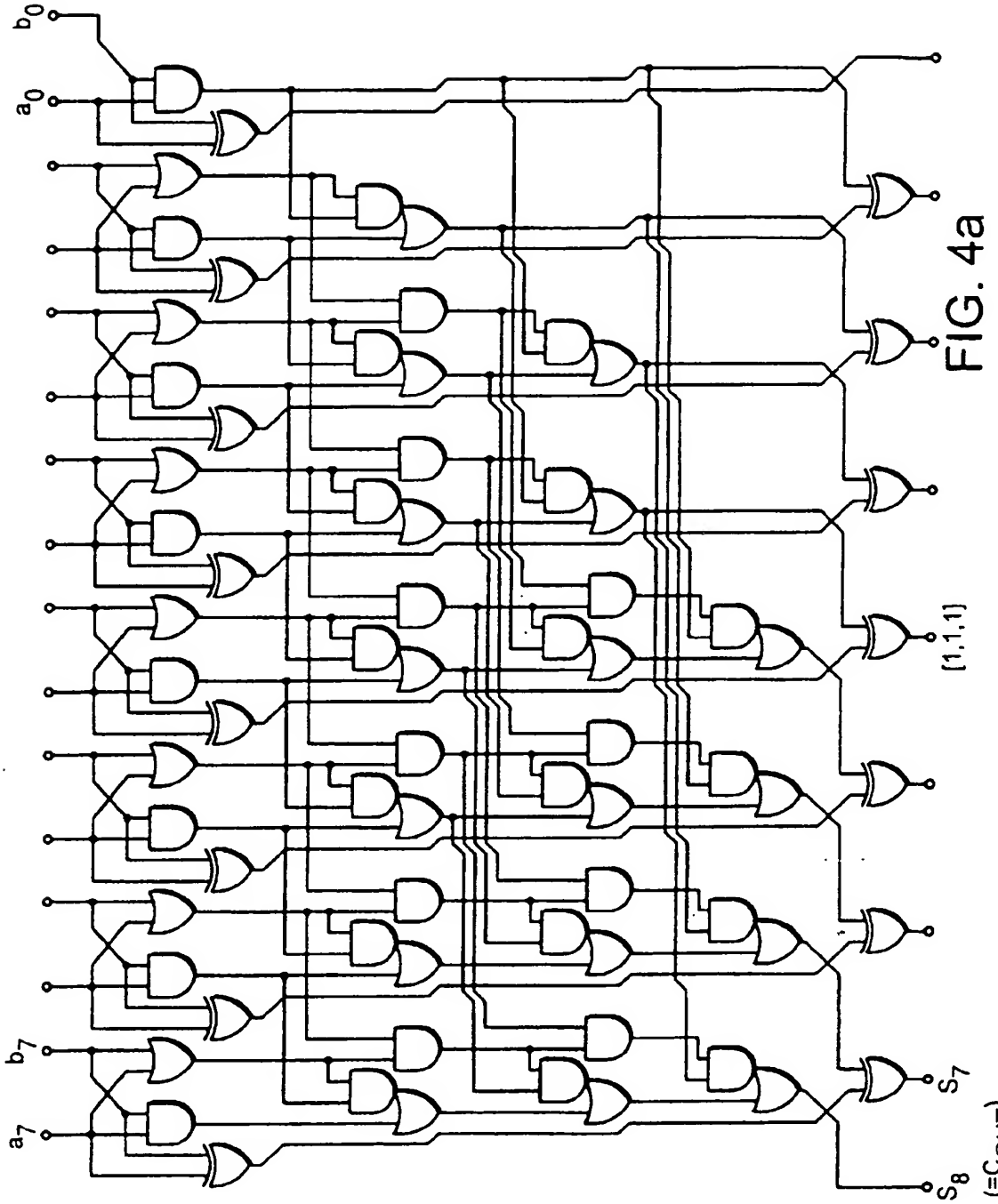


FIG. 4a

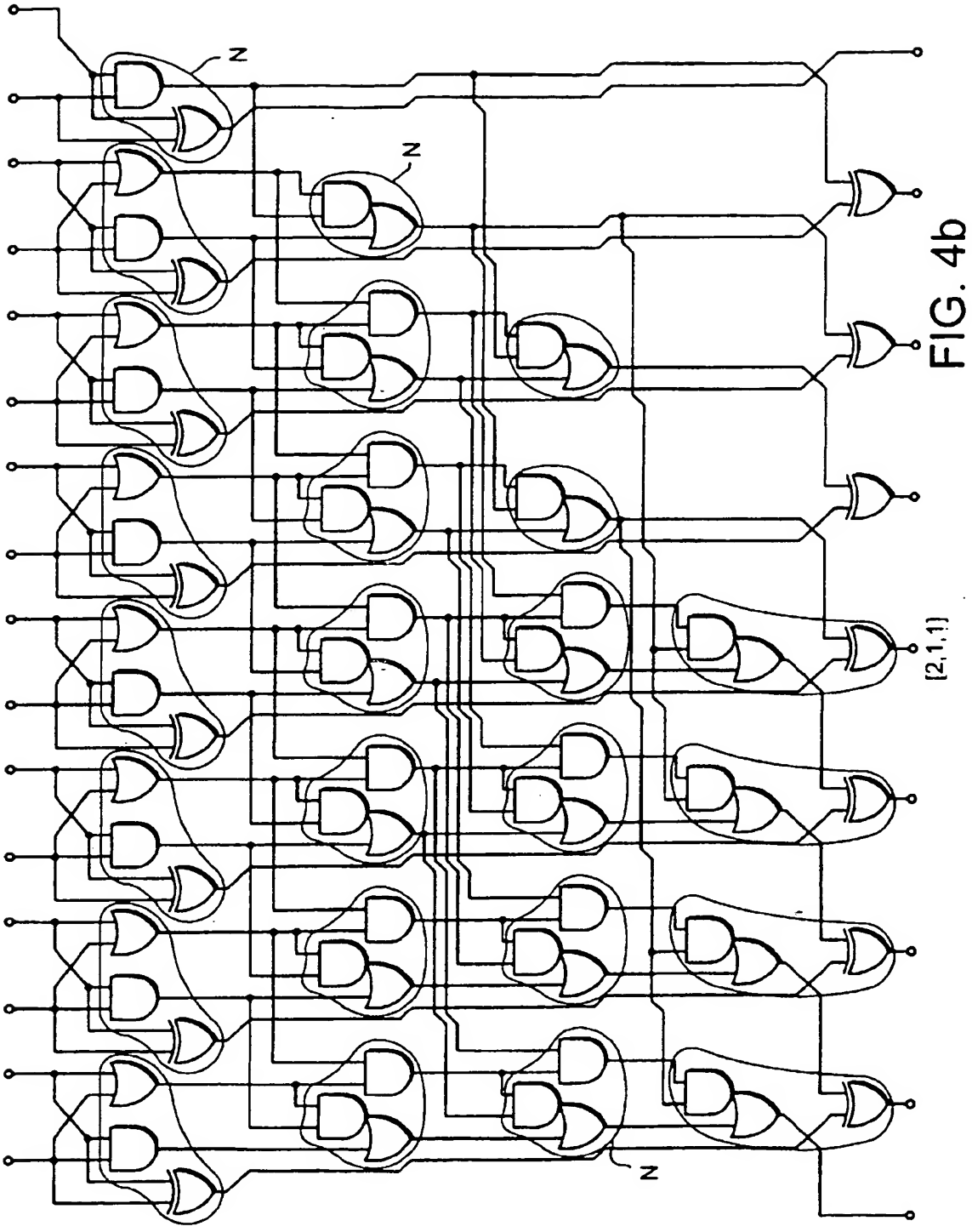


FIG. 4b

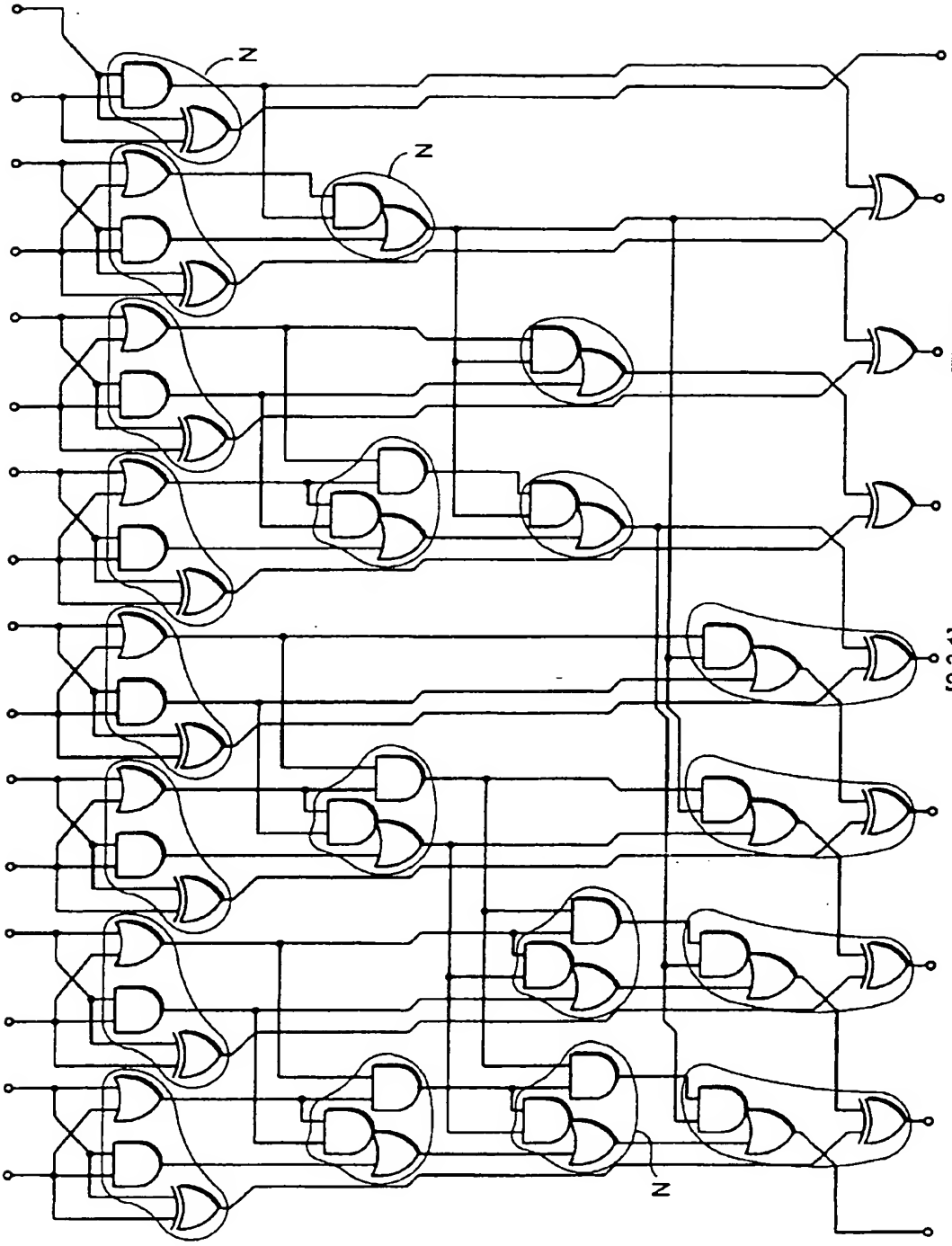


FIG. 4c

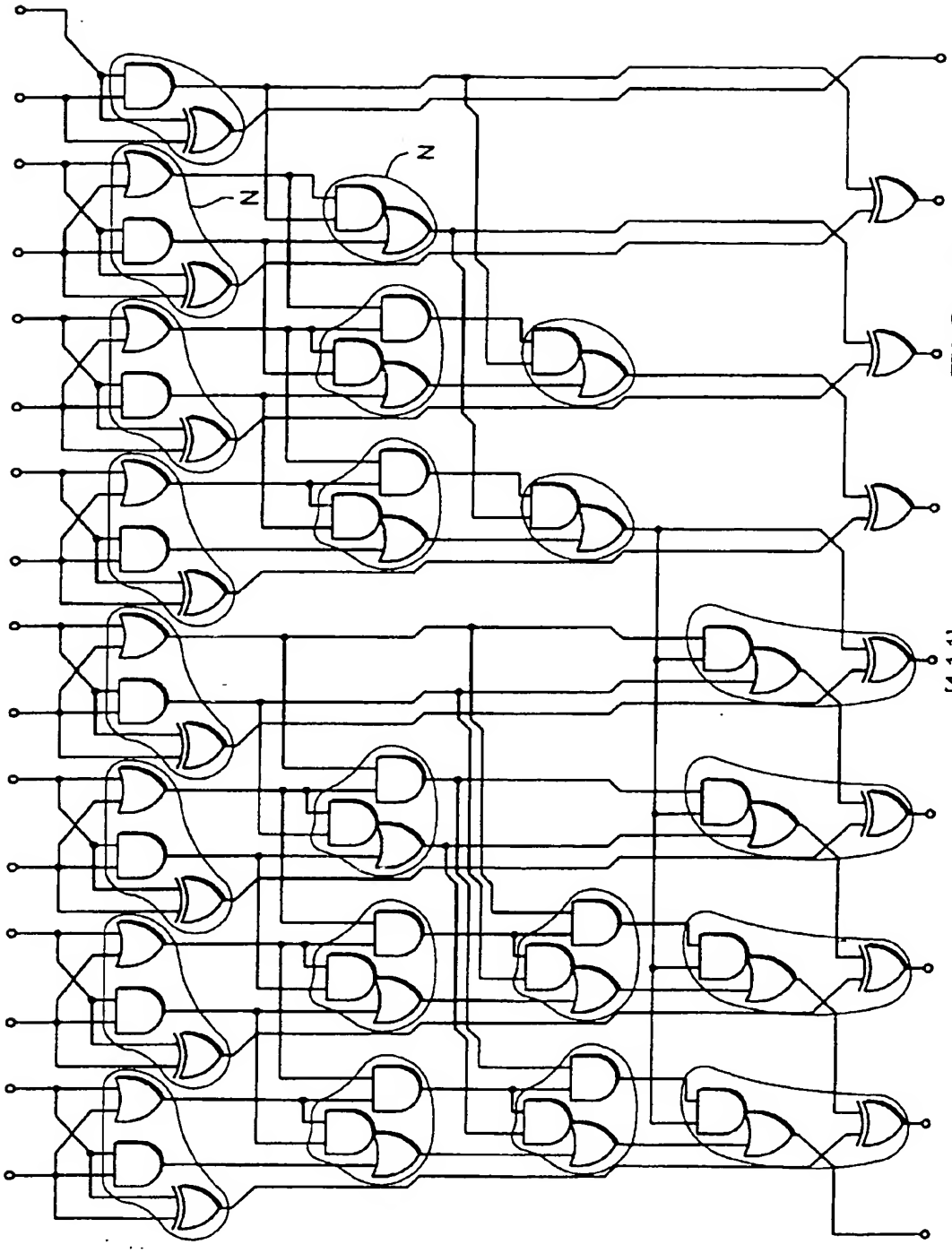
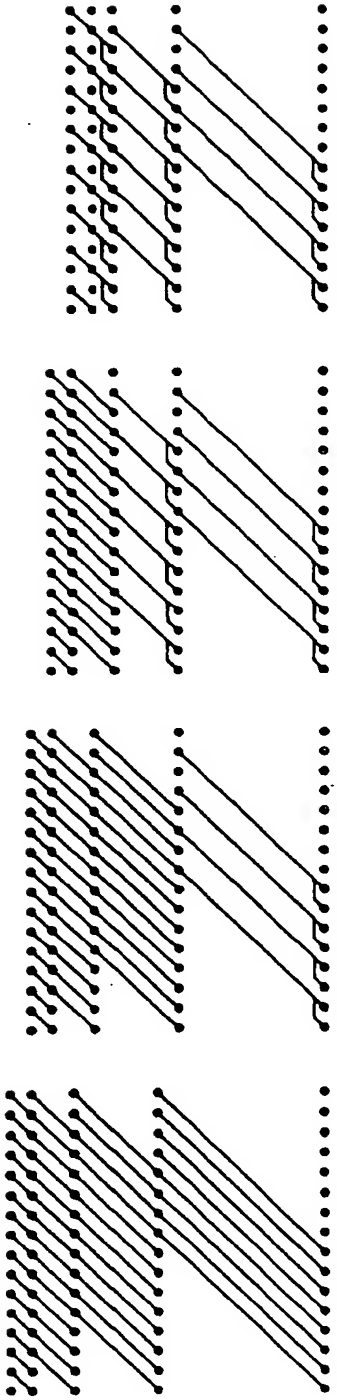


FIG. 4d



[1,1,1,1]

FIG. 5a

[2,1,1,1]

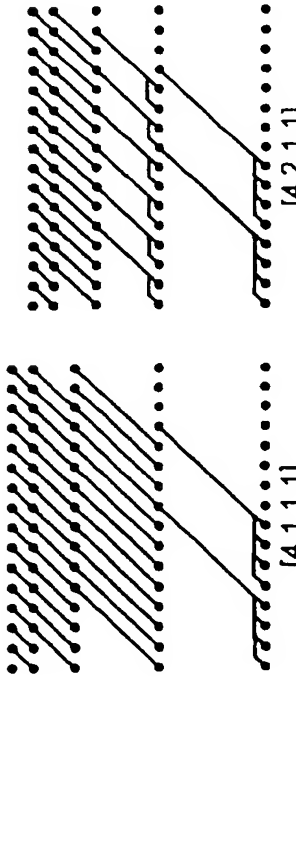
FIG. 5b

[2,2,1,1]

FIG. 5c

[2,2,2,1]

FIG. 5d



[4,,1,1,1]

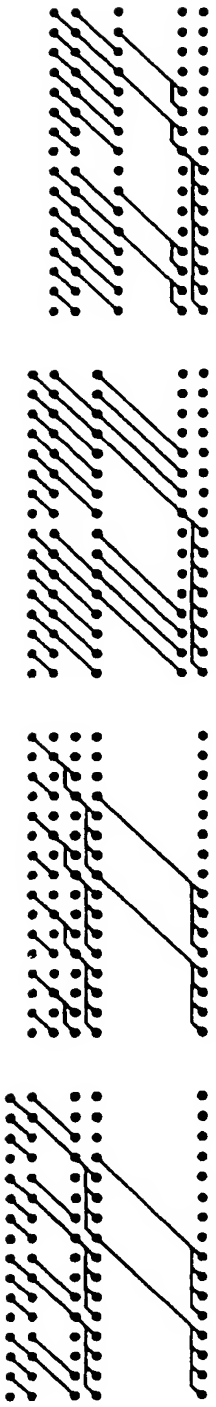
FIG. 5e

[4,2,1,1]

FIG. 5f

[4,2,2,1]

FIG. 5g



[4,4,1,1]

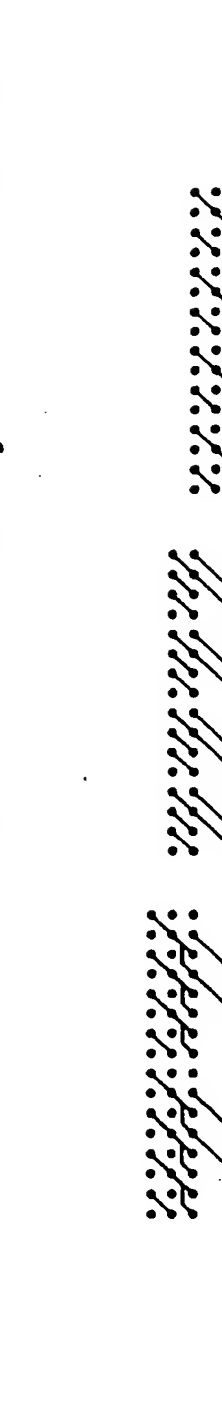
FIG. 5h

[4,4,2,1]

FIG. 5i

[8,1,1,1]

FIG. 5j



[8,2,1,1]

FIG. 5k

[8,2,2,1]

FIG. 5l

[8,4,1,1]

FIG. 5m

[8,4,2,1]

FIG. 5n

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 4339

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	KOWALCZUK J ET AL: "A new architecture for an automatic generation of fast pipelined adders" ESSCIRC '91. SEVENTEENTH EUROPEAN SOLID STATE CIRCUITS CONFERENCE. PROCEEDINGS, MILAN, ITALY, 11-13 SEPT. 1991, pages 101-104, XP002095642 1991, Milan, Italy, Tecniche Nuove, Italy * figure 3 *	1,10	G06F7/50
A	BEAUMONT-SMITH A ET AL: "A GaAs 32-bit adder" PROCEEDINGS. 13TH IEEE SYMPOSIUM ON COMPUTER ARITHMETIC (CAT. NO.97CB36091), ASILOMAR, CA, USA, 6-9 JULY 1997, pages 10-17, XP002095643 ISBN 0-8186-7846-1, 1997, IEEE Computer Society Press, Los Alamitos, CA, USA * figures 1-5 *	1,10	
A	EP 0 707 262 A (IBM) 17 April 1996 (1996-04-17) * figure 3 *	1,10	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G06F
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	1 November 1999	Verhoof, P

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